AMENDMENTS TO THE SPECIFICATION

Please replace the Title with the following: SEMICONDUCTOR DEVICE HAVING A NON-VOLATILE MEMORY TRANSISTOR.

Please replace Paragraph [0004] of the specification with the following:

[0004] A third dielectric layer 74 is formed on the floating gate 72. The third dielectric layer 74 is composed of a dielectric layer that is formed by selectively oxidizing part of a polysilicon layer that becomes to be the floating gate 72. In other words, the third dielectric layer ~~72~~ 74 has a structure in which the film thickness thereof becomes thinner from its center toward both of its end sections, as shown in Fig. 18. As a result, upper edge sections 720 of the floating gate 72 form sharp edges, such that an electric field concentration is apt to occur at the upper edge sections 720. An interlayer dielectric layer 240 is formed on the silicon substrate 10. The interlayer dielectric layer 240 is generally composed only of a silicon oxide layer. A through hole 246 is formed in a specified region of the interlayer dielectric layer 240. The through hole 246 is filled ~~which~~ with a conductive material to form a contact layer 32. A wiring layer 30 that is electrically connected to the contact layer 32 is formed on the interlayer dielectric layer 240.